FERMI NATIONAL ACCELERATOR LABORATORY

Design and Implementation of a RF Wide Band Phase Detector enhanced with signal monitoring capabilities

Research project report elaborated as part of the Summer Internship in Science and Technology (SIST) program

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Abstract

This paper describes the implementation and design of a RF wideband phase detector enhanced with diagnostic capabilities that enable better signal monitoring. The Booster RF is a dynamic system in the sense that the RF signal fed to the accelerating cavities sweeps from 37 to 53 MHz in about 35.5ms. Therefore, the resonant frequency of the cavities must change accordingly to maintain maximum accelerating voltage to the proton beam. A phase detector is used to measure the phase relationship between the RF signal and the cavities resonant frequency. The error signal produced by the phase detector is then used in a feedback loop to keep the Booster high-level RF system tuned correctly. For troubleshooting and monitoring purposes, it is often required or preferable to examine the RF signal fed into the system in order to detect or notice any disturbance, or defaults in it. As a result, we elaborated a RF phase detector design that includes additional useful features. The scope of our work was designing and building the module as a device capable of fitting in the RF system for an accurate operation.

Introduction

A phase detector is important for the purpose of directly measuring the phase relationship between the cathode and the anode of the Power Amplifier supplying RF power to the RF cavities. The resonant frequency of the cavity is controlled via three ferrite tuners that are located on the sides and bottom of the cavity. Injecting a certain amount of current through the ferrite tuners changes the inductance of the cavity, the more current the less inductance. The resonant frequency is giving by $\omega_r = {}^{1}/_{\sqrt{LC}}$

where L is the inductance and C the capacitance of the cavity. It can be seen from this equation that as the inductance decreases the resonant frequency increases. A programmable Ferrite Bias Supply (Bias Supply) is used to inject current into the ferrite tuners. The Bias Supply is a voltage controlled current source. A predetermined voltage program (bias curve) is generated and fed to the Bias Supply. In theory the Bias Supply then produces the right amount of current to the ferrite tuners to keep the cavity at resonance with the sweeping frequency of the RF signal, in other words, the resonant frequency of the cavity also sweeps from 37-53MHz. This means that if the cavity is tuned correctly, then, the RF signal in the cavity will be in Phase with the RF signal being fed to it via the RF Power Amplifier (PA). The RF signal fed to the PA is monitored at the Cathode of the PA and the RF signal to the cavity is monitored at the Anode of the PA. If the cavity is not tuned correctly the impedance of the cavity will have a resistive and

reactive component to it resulting in a RF voltage vector that is at a phase angle Ø with respect to the applied RF signal. How do we bring the signals back in phase? The Anode signal is brought back in phase with the Cathode signal by the use of a phase detector. The phase detector will generate an error signal when it detects a phase difference between the Anode and Cathode RF signals. This error signal is then fed back to the Bias Supply and multiplied into the Bias Curve. The Bias supply will supply more or less current to the ferrite tuners until the phase angle between the Anode and Cathode signal goes to zero. This keeps the cavity tuned to the applied sweeping RF signal.

Our project was concerned with the design of a prototype of one phase detector module that could integrate not only a phase detector's functionalities but also three other useful capabilities enabling the visualization and monitoring of the input signals. The functionalities of our system included:

1- Phase detection between two signals, with components chosen to be optimal between 30-60MHz.

2- Monitoring ports allowing the raw RF signals to be viewed as they come in.

3- Envelope detection that could be visualized as voltage signal matching input power signals.

4- Frequency-to-voltage conversion available through output voltage that can be plotted as function of the frequency.

1. System situation: an overview of the Cavity tuning system

The application of RF (Radio Frequency) energy accelerates the Booster beam. The beam receives this energy as it passes through each of the 18 ferrite-tuned resonators, commonly referred to as "cavities," located around the Booster ring. A 100 kW PA Power Amplifier) drives each cavity. A set of "low level" RF waveforms drives the "high level" RF which is made up of amplifiers, cavities, and associated hardware.
There are three distinct phases to the accelerating cycle:

1- Injection, capture, and bunching over the first 2 msec.

2- Acceleration, which lasts about 29 msec.

3- Phase locking to the Main Injector and extraction, which occurs over the final 2.5 msec. (If phase locking to the Main Injector is not desired, then the frequency trigger is withheld, and the acceleration sequence proceeds the rest of the way to extraction).

During acceleration the RF frequency must follow the change in velocity in the protons; the frequency at injection is roughly 37.86 MHz and increases to 52.81 MHz at extraction time.

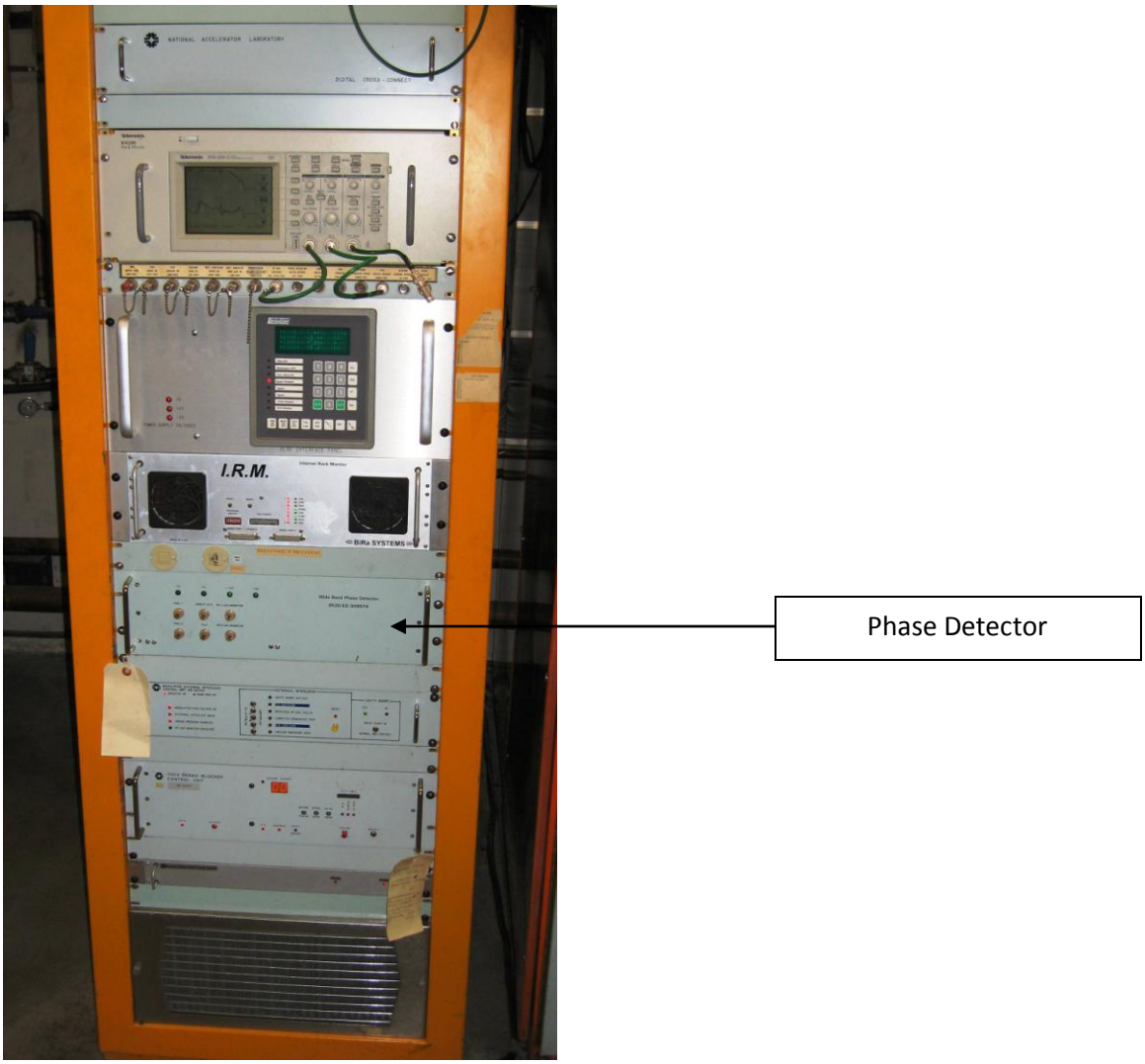

Figure 1: Phase detector in use mounted in rack

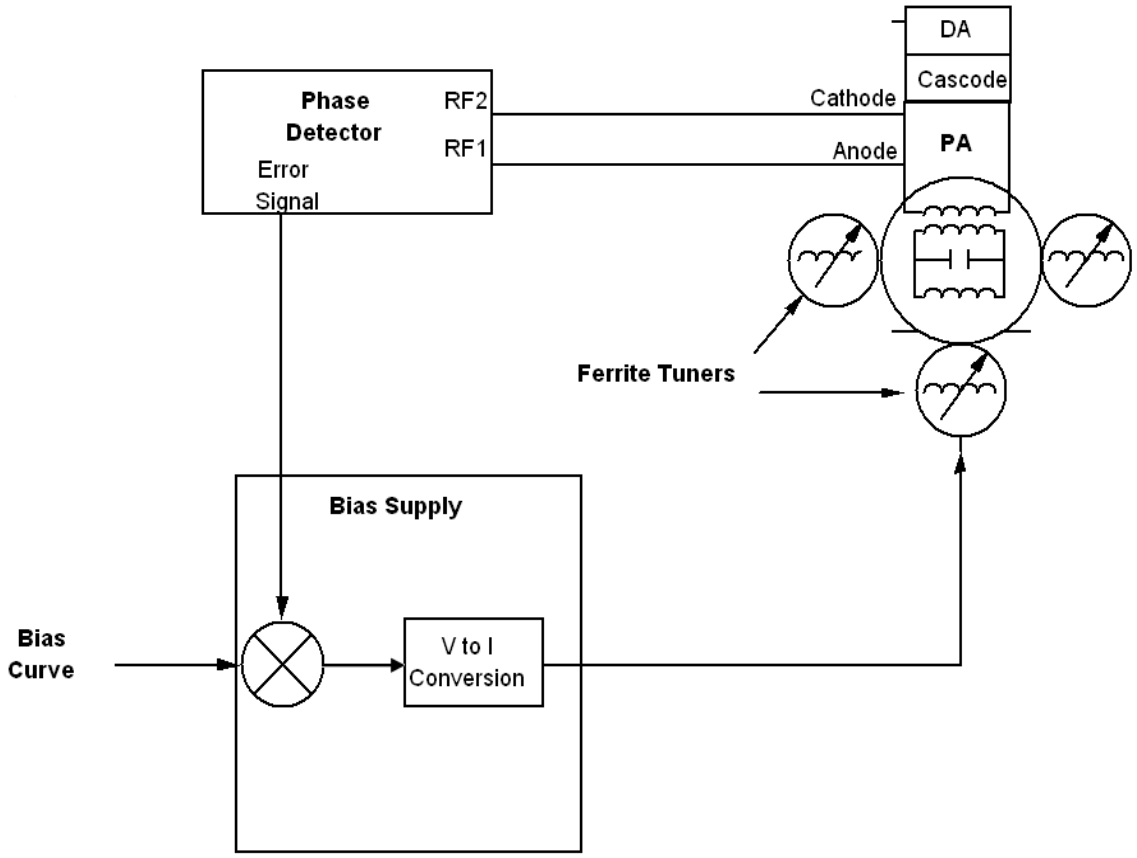

Figure 2: Booster RF cavity tuning

2. Description and theory of operation

2.1. General description

2.1.1. How mixers work?

The basic concept upon which phase detection rests is that the application of two identical frequency, constant amplitude signals to a mixer, results in a dc output which is proportional to the phase difference between the two signals. While it is true that even a single diode can be used as a mixer, most phase detectors involve the use of double balanced mixers. With this in mind, the theory presented here assumes that a double balanced mixer is being used. Figure 3 is a schematic of a typical double balanced, four diode ring mixer.

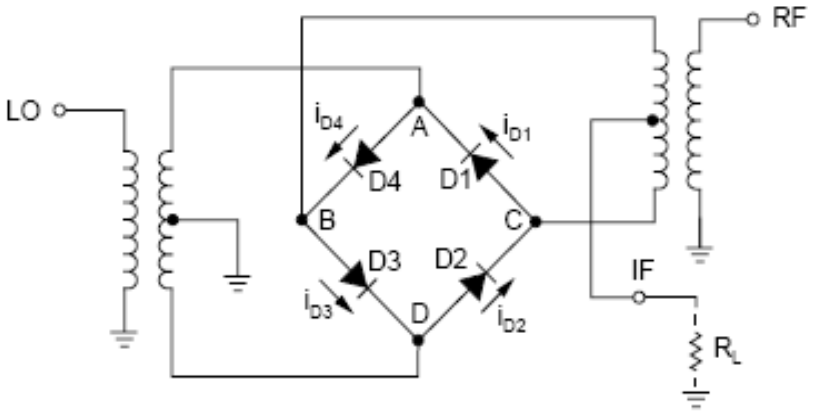

Figure 3: A typical double-balanced mixer

The voltage at the secondary of the LO transformer causes currents to flow through diode pair D1, D2 or D3, D4, depending on polarity. The DC voltage at B or C is held at virtual ground potential by the voltage divider action of the conducting diode pair. The diode pairs (D1, D2 and D3 D4) alternate conduction, causing the ends of the RF transformer's secondary winding (B and C) to be alternately at ground potential, switching at a rate equal to the frequency of the input signal to the LO port. The instantaneous voltage at the IF port is determined by:

the level and polarity of the instantaneous voltage at the RF transformer' s secondary winding; and

which terminal of the secondary is at ground potential at that instant.

The output at the IF port contains the sum and difference of the frequencies of the signals input to the LO and RF ports. If the RF and LO signals have identical frequencies, then their difference is zero Hz, or dc, which is the desired output for a phase detector. Their sum, which is twice the input frequency, can be selectively filtered out if it is not already beyond the frequency response of the IF port.

2.1.2. Mathematical description

In order to demonstrate mixer operation mathematically, we need to first look at the mixing process as it occurs in each diode. The conductance waveform for the diode can

be expressed in terms of the local oscillator frequency and its phase angle as shown below:

$$G(\ _L t \quad _L) \quad \sum_n g_n \exp(j(n(w_L t \quad _L))) \tag{1}$$

where: $_L$ *frequency of the LO signal*

$_L$ *phase angle of the LO signal*

g_n *const.*

Applying an RF signal, the small signal voltage across the diode is $V_{RF}(\ _L t \quad _R)$, which results in a diode current waveform of:

$$i_D \quad G(\ _L t \quad _L) V_{RF}(\ _R t \quad _R) \tag{2}$$

If V_{RF} is expressed as:

$$V_{RF}(\ _R t \quad _R) \quad \sum_m v_m \exp(j(m(\ _R t \quad _R))) \tag{3}$$

then combining equations (1), (2), and (3) yields

$$i_D \quad \sum_{n,m} g_n v_m \exp(j(n(\ _L t \quad _L) \quad m(\ _R t \quad _R))) \tag{4}$$

Assuming a load resistance R, if we rewrite the exponential in equation (7) in trigonometric form, keeping only the real part, the result is

$$V_{IF} \quad 2Rg_{\ 1} v_{R\ 1} \cos(\quad _L \quad _R) \tag{5}$$

or

$$V_{IF} \quad 2Rg_{\ 1} v_{R\ 1} \cos(\quad) \tag{6}$$

which indicates that the voltage at the IF port will be dc and will vary as the cosine of the phase difference between the LO and RF signals.

3. Actual Design and Implications

3.1. Main Design Specifications

Our phase detector module (board) has been designed according to a certain number of specifications regarding the RF system tuning and calibration requirements. The design was performed in such a way that voltage, current or phase requirements should be met at the front-end. These major specifications were:

-Output Phase Detector: 20Vp-p

-Output envelope detector: 0.03V/dBm

-Output voltage-to-frequency converter: linear response describing a voltage as a function of frequency with a slope of 0.1 V/MHz.

3.2. Module Overview and Description

The Wide Band Phase Detector measures the amplitude and phase relationship between two RF signals. It has two input ports, RF1 and RF2. There is a pair of monitors on both the front and back panels were the power of RF1 and RF2 can be measured. These monitors are labeled RF1 LOG Monitor and RF2 LOG Monitor.

There are two monitors to measure the phase relationship between RF1 and RF2. These monitors are DIRECT OUT and Eout and can be monitored from both the front and rear panels. DIRECT OUT gives a phase error signal of 1V/45˚. Eout gives a phase error signal of 1V/9˚. And we have the Vlog and Freq.-to-Voltage terminals for both of the RF signal where diagnostic data can be viewed. The phase detector also has other features like TRIG1, TRIG2 and INHIBIT which can be used or bypassed internally by changing a shorting connector. The module can be active all the time or active for a specific time.

3.3. Main components description

- The SRA-1(Double-Balanced Mixer)

This component is a DBM (Double Balanced Mixer) which is as seen earlier, a DBM is an ideal device for phase detection since it offers high isolation between all three ports, the reference (LO), input signal (RF), and output (IF). From a phase detector perspective, when two signals of identical frequency but different phase are applied to the inputs of

a balanced mixer, the output at the IF port will be dc voltage proportional to the phase difference.

- The PSC-2-1 (Power Splitter)

It's a passive device which accepts an input signal and delivers multiple output signals with specific phase and amplitude characteristics. The PSC-2-1 is a two way 0^{o} which means we have a 0^{o} relationship between any two output signals and a high isolation between each of those signals.

- The AD3806 (Log Amp)

It's an IC logarithmic amplifier which produce an output that is proportional to the common logarithm of the input signal amplitude; this response is described to be linear-in –dB. A logarithmic amplifier essentially calculates the logarithm of an input's signal's envelope. They are therefore used to measure signal strength by converting an input signal (voltage) of wide dynamic range into its decibel equivalent.

3.4. Block Diagram of the wide band RF phase detector

The phase detector system includes two RF input signals. Our phase detector functional representation is shown is the block diagram of Figure 4.

Two RF signals of equal frequency are applied to RF1 and RF2 inputs on the back panel. Each of the RF signals passes through a two-way 90˚-power splitter, which are U1 and U3. RF1 is kept at 0˚ and RF2 is shifted 90˚ by the splitter U3.

The signals are then fed into a pair of AD8306 Limiting-Logarithmic Amplifiers, U2 and U4. The output VLOG of the Amplifiers provide an accurate logarithmic measure of the RF signals and can be monitored on the back or front panel labeled RF 1 Log Monitor and RF 2 Log Monitor. The Amplifier also provides a limiter output, LMHI and LMLO where the incoming sine wave RF signal is converted into a square wave of fixed amplitude. This removes the amplitude difference between the two signals while retaining their phase difference Ø.

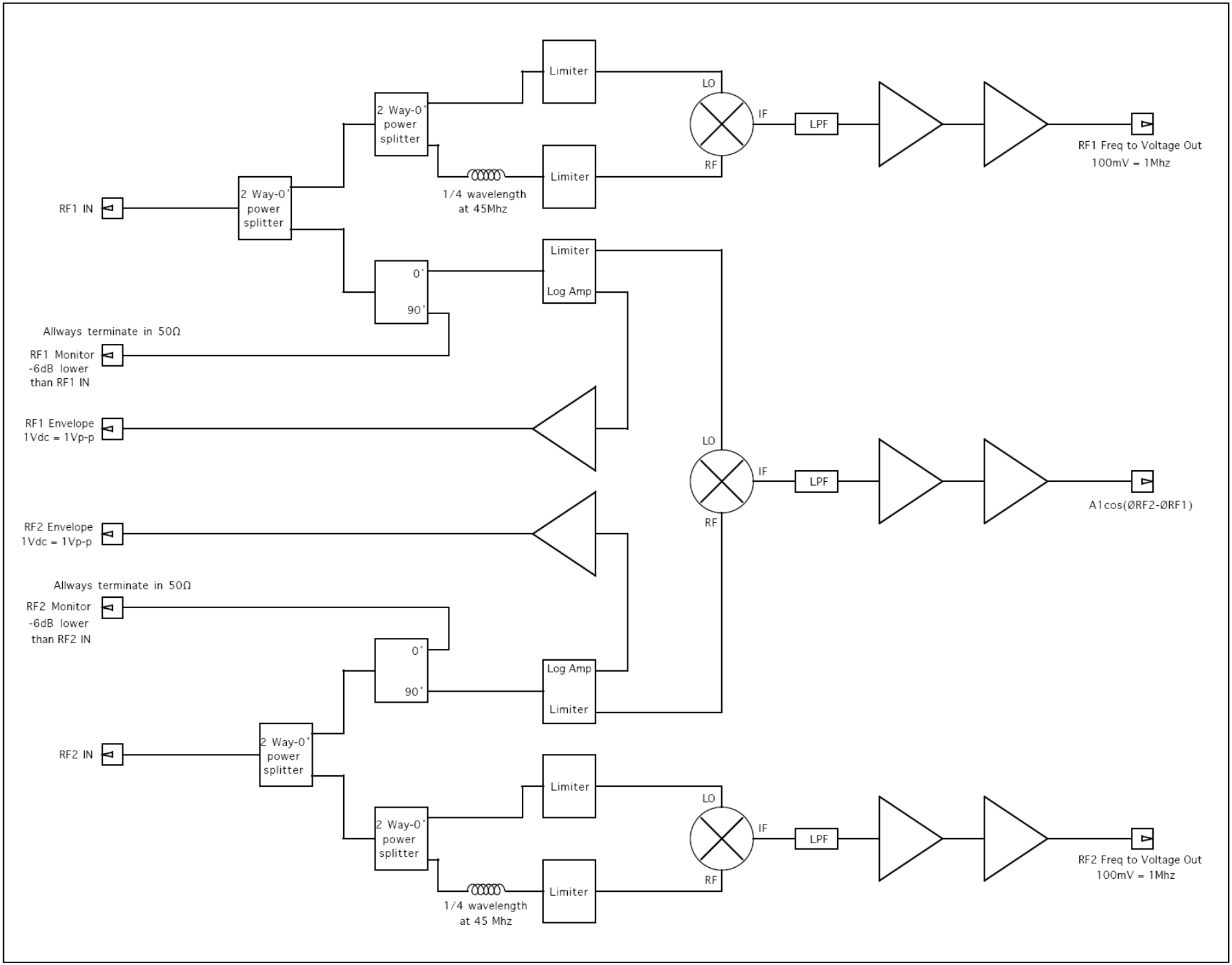

Figure 4: System block diagram

Since the limiter output of the AD8306 has a dc component it must be coupled out before going into the mixer. Impedance matching transformers T1 and T2 eliminates the dc component.

The Phase Detector is designed around the SRA-1 mixer from Mini-Circuits, U5. The mixer has two inputs, LO and RF, and an output IF. The output **IF** will be of the form

$$A1\cos[(\omega_{\mathrm{LO}}-\omega_{\mathrm{RF}})\mathrm{t}-(\emptyset_{\mathrm{LO}}-\emptyset_{\mathrm{RF}})]+A2\cos[(\omega_{\mathrm{LO}}-\omega_{\mathrm{RF}})\mathrm{t}-(\emptyset_{\mathrm{LO}}-\emptyset_{\mathrm{RF}})] + [higher\ order\ terms] \quad (7)$$

Where A1 and A2 are the peak amplitude of the LO and RF signals, WLO and WRF are the signal frequencies and ØLO and ØRF are the signals phase. If the two signals have

the same frequency, $\omega_{RF}=\omega_{LO}$, the term $(\omega_{LO}-\omega_{RF})$ will disappear and **IF** will only be a function of

$$A1\cos(\emptyset_{LO}-\emptyset_{RF})+A2\cos(2wt)+[higher\ frequency\ terms] \quad (8)$$

The Low Pass filter following the mixer will eliminate the 2wt and higher frequency terms so that **IF** has the form $IF=Kd\cos(\emptyset_{LO}-\emptyset_{RF})$.

The amplitudes of the two signals must remain constant for they can add dc errors on the IF output. Also, one of the signals must be shifted -90˚ so when the signals are in phase, coming into the Phase Detector, the output IF will be 0-volts.

The first stage of the Phase Detector is to shift one of the signals by -90˚. Both signals are fed into a 2 Way-90˚ power Combiner/Divider. RF2 is shifted -90˚ with respect to RF1. This is done so the term $\cos(\emptyset_{LO}-\emptyset_{RF})=0$ when the two input signal are in phase coming into the phase detector. After the phase shift the two RF signals are fed into a limiter. The limiter provides a square wave RF signal with constant amplitude. This ensures that the output of the mixer, **IF**, is a function of the phase difference $(\emptyset_{LO}+\emptyset_{RF})$ of the two RF signals only and not of their amplitudes changes.

4. Experimental Design Approach

- Designing the Phase Detector (section) circuitry:

The RF signal is generated by a cavity resonator centered at the RF frequency. It is followed by a limiter (AVC) that provides a constant RF level at its output so that the phase measurement is insensitive to the beam intensity.

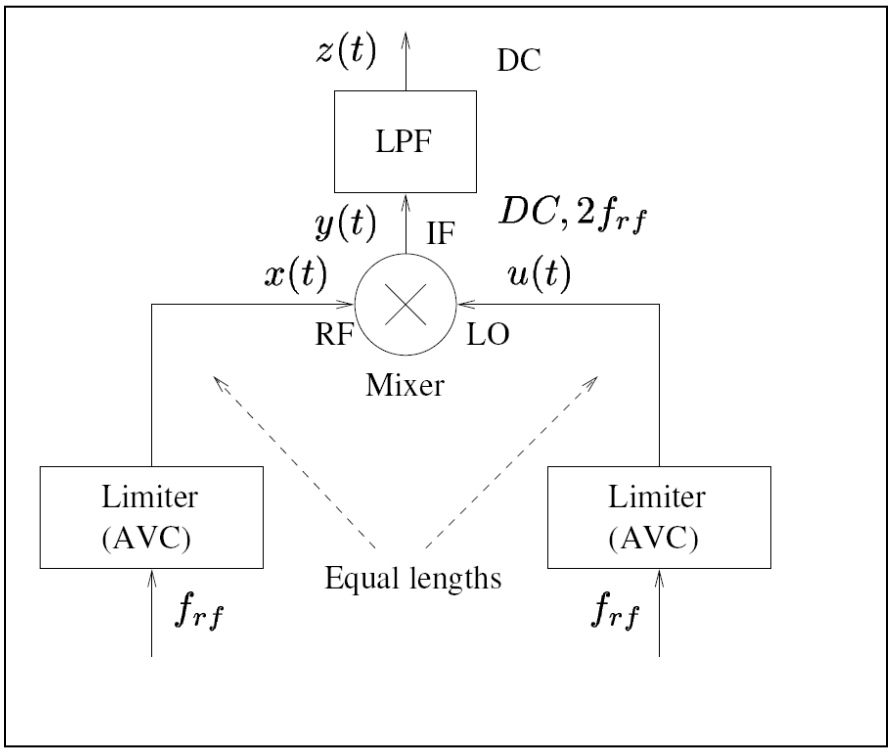

Figure 5: Processing at the RF frequency

The design and building of the phase detector section circuit on the board involved the selection of appropriate filters, amplifiers, buffers along with a correct and exact construction of different circuits involving ICs. The phase detector circuitry described by the path followed by the signal from the RF input connector to the voltage output terminal, mainly includes filters, power splitters, the SRA-1 mixer, and the AD8306 amplifier. A PIF-40 (bandpass filter) is mounted at the very beginning of the signal path in order to get rid of undesirable harmonics. The filter is followed by a 2 way-0^{o} power splitter (PSC-2-1) that provides two output signals among which one is used to for the phase detector part. This signal goes into another power splitter (PSCQ-2-60) before it

gets amplified by the AD8306 which is a Log-amp demodulator. The AD8306 is mounted in its limiter configuration providing and output signal at pin 13 which is fed into the DBM. Since two RF signal are supposed to be fed into the DBM, another input RF signal goes from the RF2 input to the DBM which then generates a voltage at the output that we amplify by using two OPA637BM and a buffer BUF634T.

- Designing the frequency-to-voltage converter:

The frequency to voltage section circuitry mainly includes AD8306 amplifiers, one SRA-1 and also a series of amplifiers and buffers. The frequency-to-voltage converter is aimed at providing a voltage function that will match with a certain range of frequency as it changes. The frequency-to-voltage converter section circuit features essentially the AD8306, the SRA-1, the OPA637 amplifier and the BUF634T. The same input RF signal that is used for operating the frequency-to-voltage converter which description is almost similar to the phase detector sector, excluded the fact that the signal picked up at the output of the low-pass filter PLP-10.7, is processed in a different way to generate a frequency-voltage function that will inform us about an exact frequency at which a problem occurs. With the signal extracted at the output of the filter, we generate a plot representing the frequency-vs-voltage characteristic.

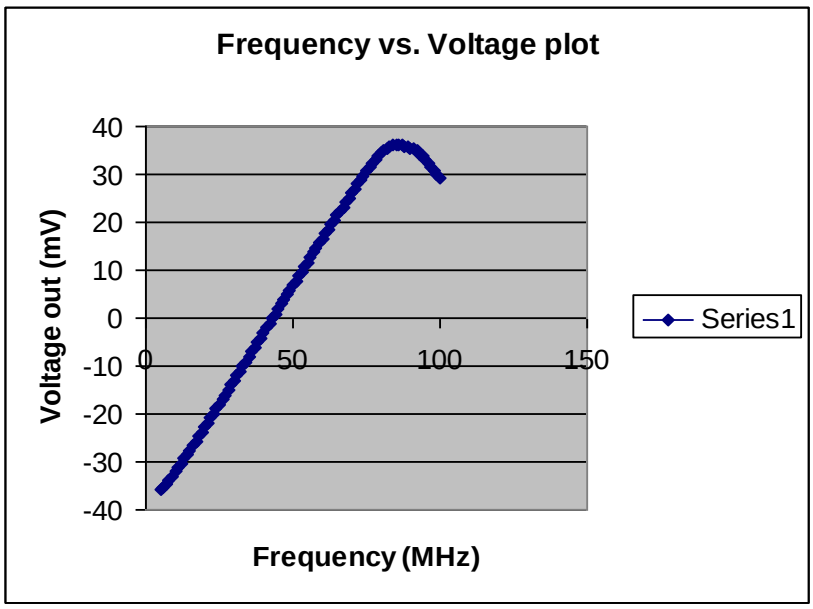

Figure 6: Plot of Frequency vs. voltage characteristic

This plot describes a linear voltage response between 5 and 87MHz which is an optimal or suitable frequency range for us to perform a voltage in order to get exactly a frequency-to-voltage characteristic that will have a slope of 0.1 meaning that at a frequency value of 37MHz for instance, we should have a voltage value of 3.7V. Two amplifiers (the OPA627 and the OPA637) are used to realize this mathematical function

- Designing the envelope detector

The envelope detector concept lays in the idea to provide an envelope signal representing any amplitude change in the RF signal. To achieve such functionality we used principally the logarithmic voltage output signal of an AD8306. The Vlog output of the AD8306 gives an indication of the ac amplitude of the signal in the logarithmic domain. According to our specifications, we were to generate an output DC voltage that could be equivalent in amplitude to the RF input signal and if any amplitude variation occurs in the RF signal, we will be able to notice that in the envelope detector output signal. Referring to the design, we considered a reference value falling in the range of the sweeping frequencies (37MHz-53MHz). We selected for example 1Vp-p at 53MHz as an input voltage that is supposed to generate a 1Vp-p dc voltage. We approached this task by getting the Vlog output signal that we fed into an OPA627 built as a non-inverting low gain amplifier.

- Retrieving the raw signal through the monitors

In order to view the raw signal, we used the existing 2way-0^0 power splitter and collected the signal that we fed into the panels connectors that we absolutely terminated in 50Ω. As a result, the same signal coming in the RF input terminals can be viewed through the monitors.

5. Results and Discussion

Upon designing and laying down the circuits on the board, we performed a series of tests that allowed us to verify the operation of the circuits and judge or assess the accuracy of the results in comparison with the expected ones.

- The Phase detector

The phase detector was designed with a fundamental requirement which is to provide an output voltage of 20V peak-to-peak with two input RF signals having a 53MHz frequency.

- The Direct out signal: the Direct out signal is measured at the output of the first OPA637 after the mixer and the filter. This signal which is always active represents a voltage value of 4Vp-p and a phase value of 1V/45^{o}. Figure 7 shows a representation of the Direct out signal generated from an oscilloscope.

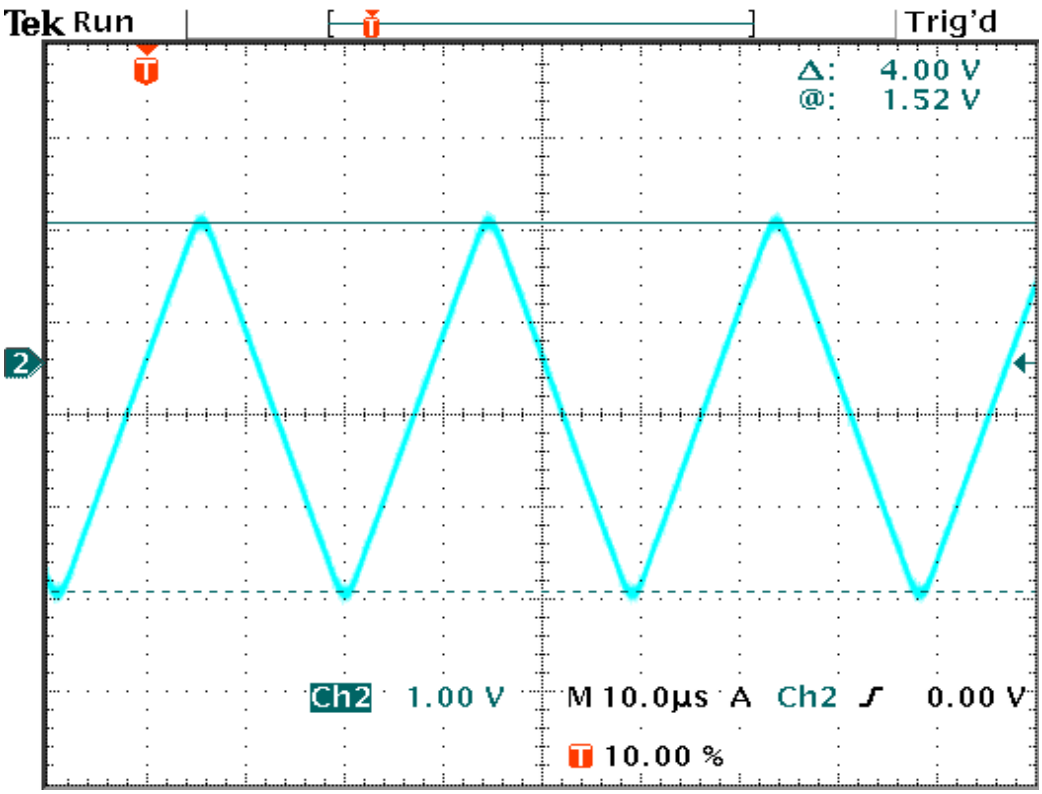

Figure 7: Oscilloscope generated plot of the Direct out voltage

- The E out voltage: this voltage is in fact the actual phase detector voltage output with a voltage of 20Vp-p and a phase value of 1V/90^{o} that will be changing as long as the input signal will be experiencing some changes. The plot in Figure 8 shows us the scope generated plot of this voltage.

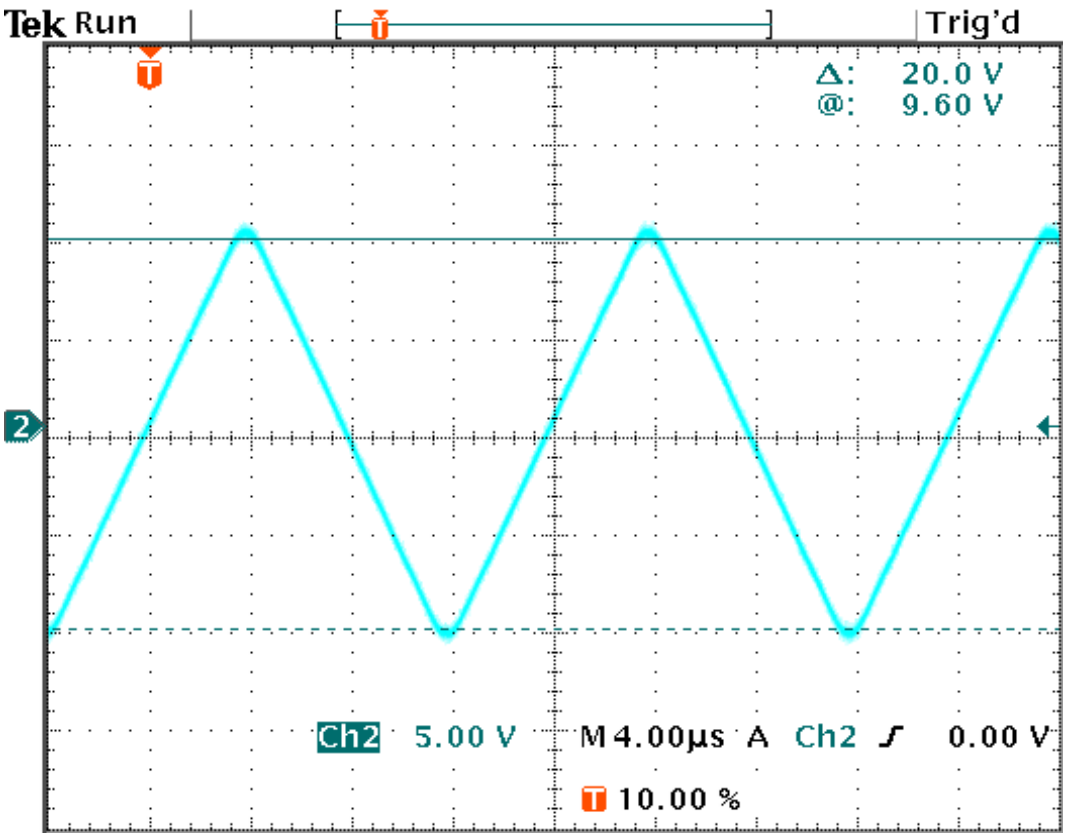

Figure 8: Oscilloscope generated plot of E out voltage

- Field testing: In order to verify exactly the operation of our device we were able to perform some tests with the device that we temporarily incorporated in the system and generated some information related to the cavity tuning signals.
  The Phase signal viewed between the anode and cathode terminals of the Power Amplifier tube describes the phase variations or fluctuations.

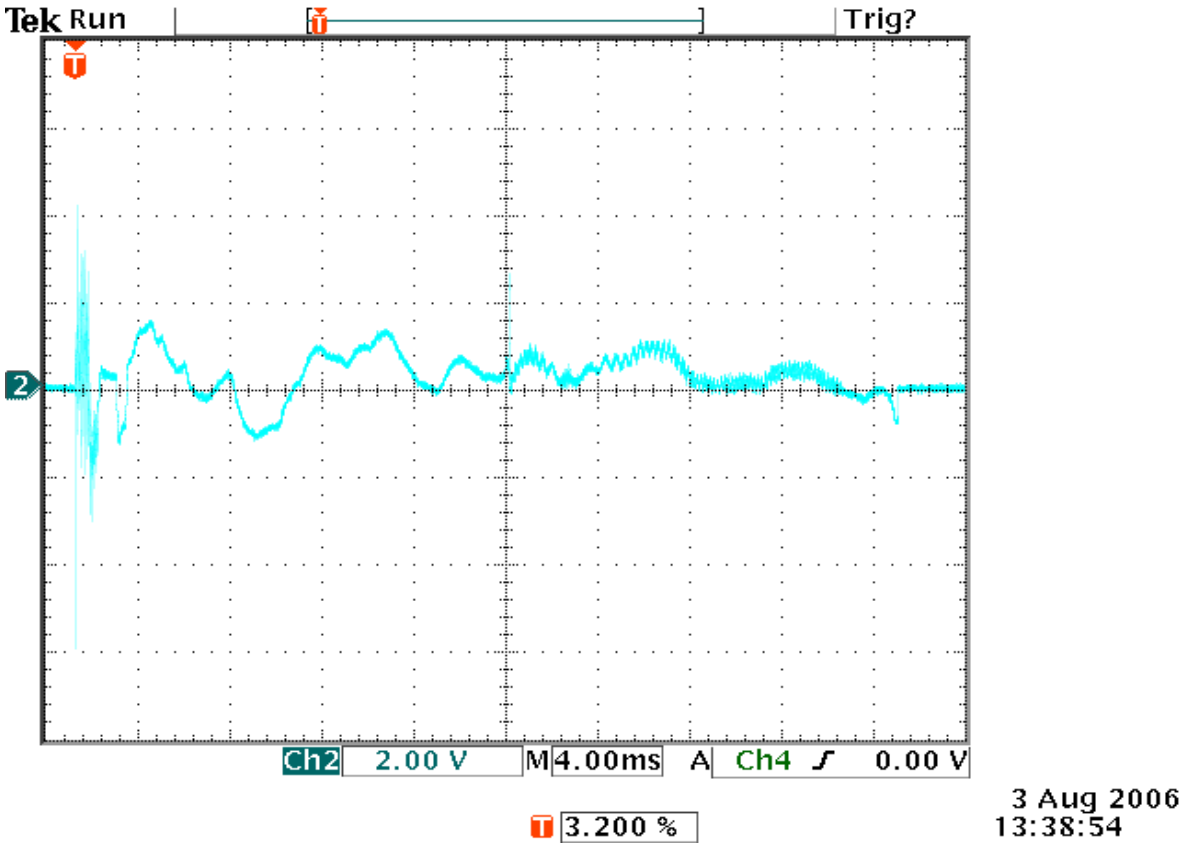

Figure 9 : Oscilloscope plot of Phase error occurring between anode and

- The frequency-to-voltage converter

  As mentioned earlier, this section of the module outputs a voltage that can interpreted into a plot of the voltage vs. the incoming frequency. After scaling the voltage coming out of the low-pass filter (PLP-10.7) we obtained a quasi linear characteristic using frequencies varying from 0 to 80MHz as input signal. Figure shows the plot of the frequency vs. voltage using a frequency generator to vary the input frequency. One important point to mention was that during the scaling process we selected in our computations, a slope of 0.1 for the curve so that we could have for example a voltage of 5.3V for a 53MHz input signal.

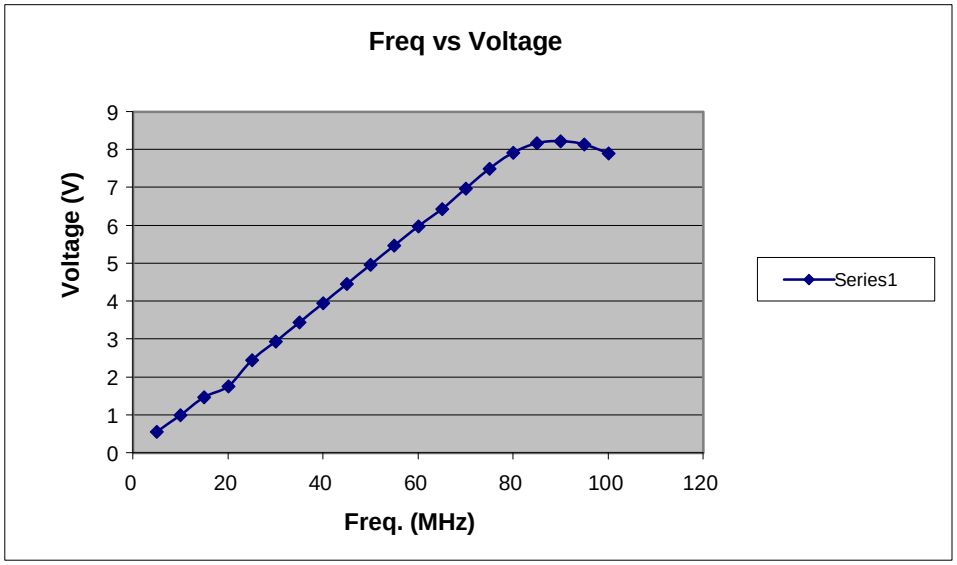

Figure 10: Graph representation of Frequency-to-Voltage converter

The following graph (Figure 11) represents the frequency sweeping occurring in the RF Booster system converted into voltage. It can be seen from this plot that the frequency sweeps from 37MHz to about 53MHz displayed in voltage as 3.7V to 5.28V. We would therefore eventually be able to locate exactly at which frequency any default or distortion is occurring looking at the voltage

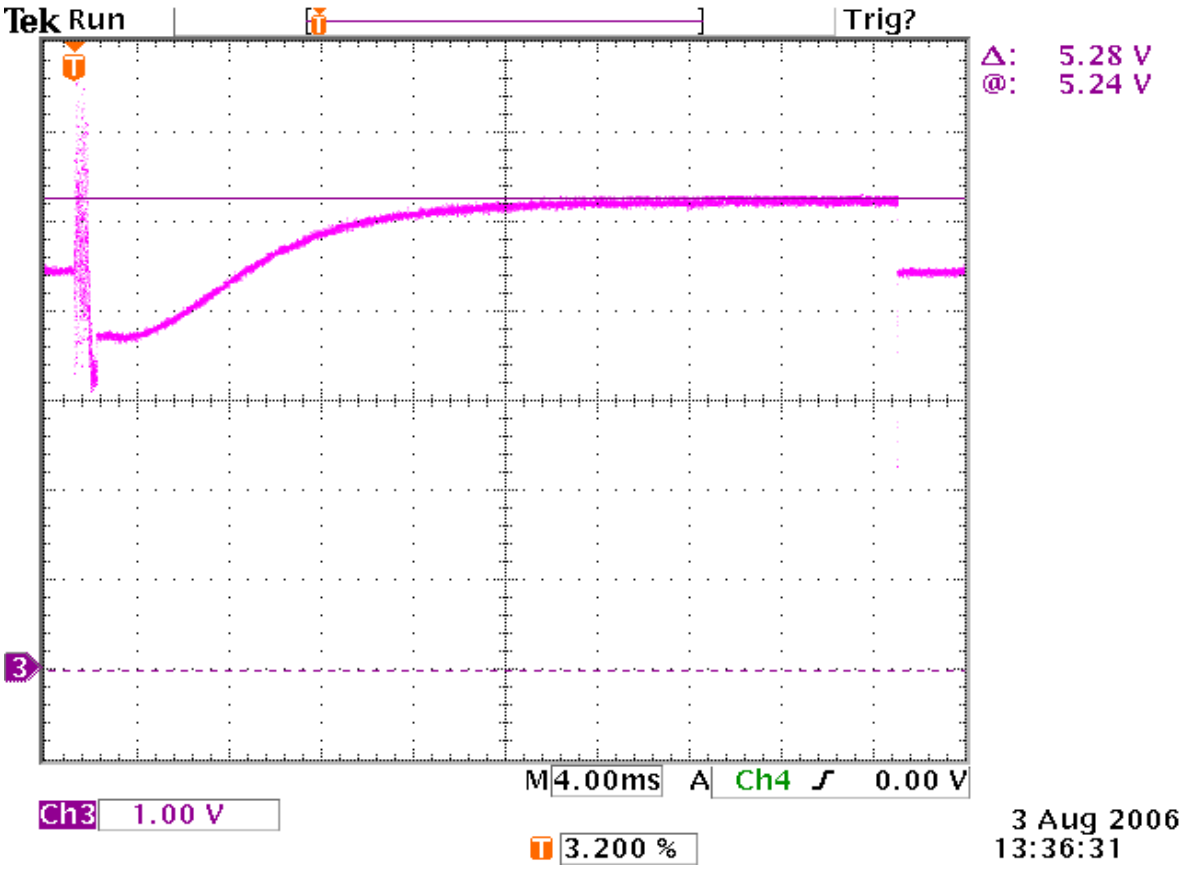

Figure 11: Oscilloscope plot of voltage converted frequency sweeping from 37 to 53MHz

- The envelope detector

  We verified the operation of the envelope detector by also generating a plot of the Vlog signal vs. the amplitude of the incoming signal (in dBm). Since the signal coming from the Vlog output was fed into an OPA627 amplifier, we were able to use voltage potentiometers in order to get rid of existing offsets so that we could manage to get an optimal output capable of matching the input signal in amplitude. We expected an output of 1Vp-p with an input signal of 1Vp-p at 53MHz. The graphic shown in Figure 12 is the plotted data of the Vlog vs. the incoming amplitude.

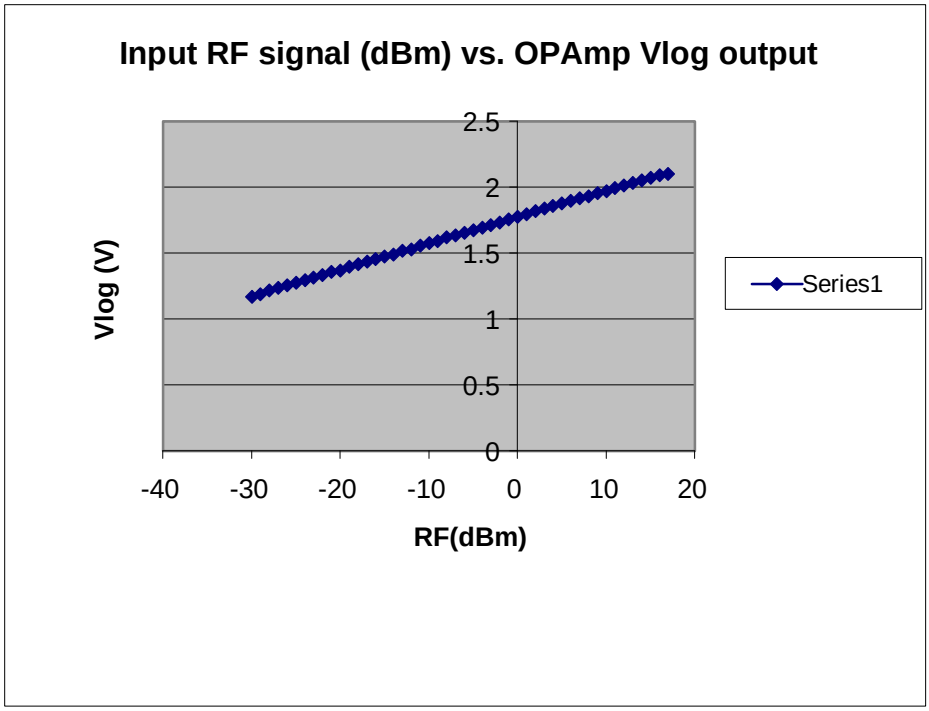

Figure 12 : Plot of envelope detector output voltage

The oscilloscope plot in the following figure represents the envelope signal of both of the anode and the cathode of the PA tube. Those output signals allow us not only to monitor the amplitude change in the RF signal, but also use it to calculate the average of the signal and use it as a feedback signal to control any amplitude change of the RF signal.

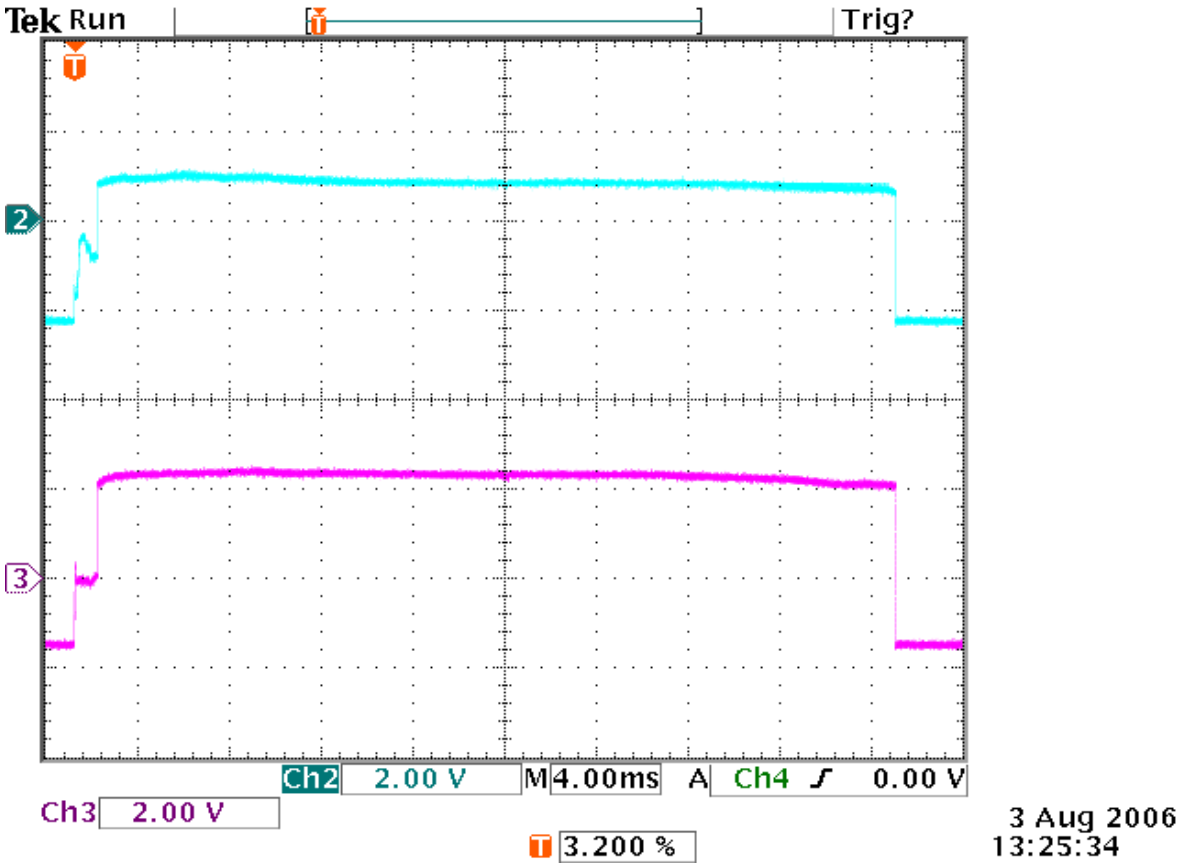

Figure 13: Envelope signals of Cathode and Anode RF power

- The Raw signal monitors

  The raw signal monitors, RF1 and RF2 monitors provided us with the input raw signal that we visualized on the oscilloscope first using the frequency generator signals and then using the cavity tuning signals.

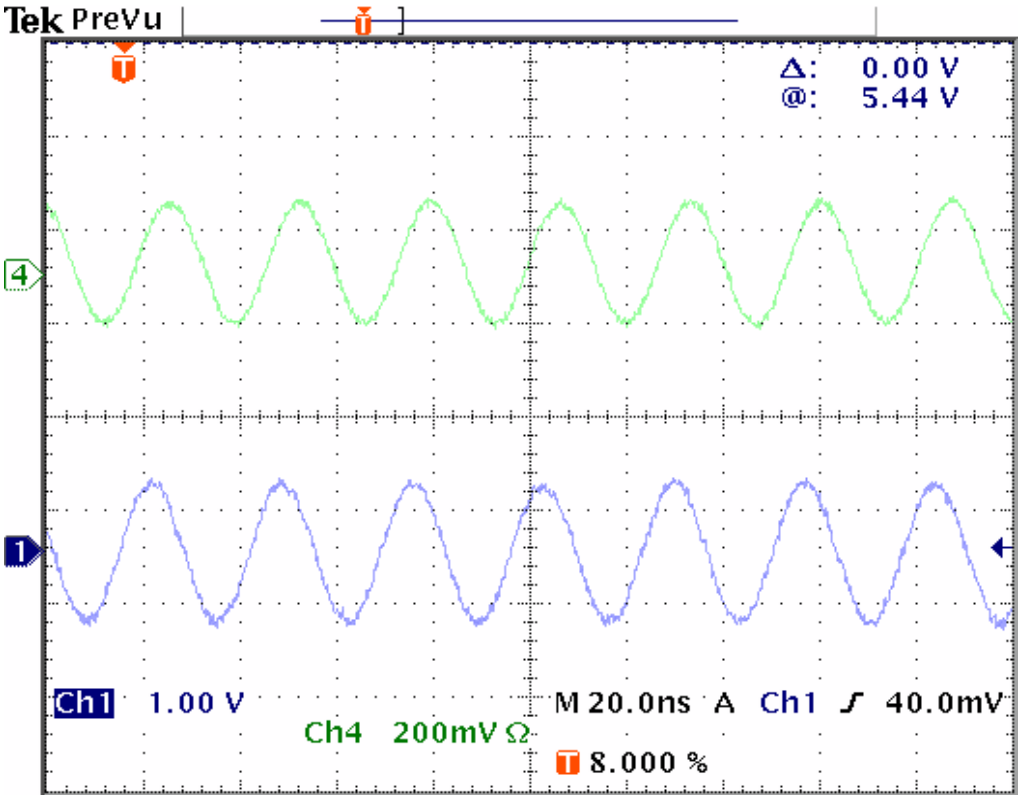

Figure 14: Signal generator monitored signal through RF1 monitor

The raw RF input signal coming from the anode (channel 2) and from the cathode (channel 3)

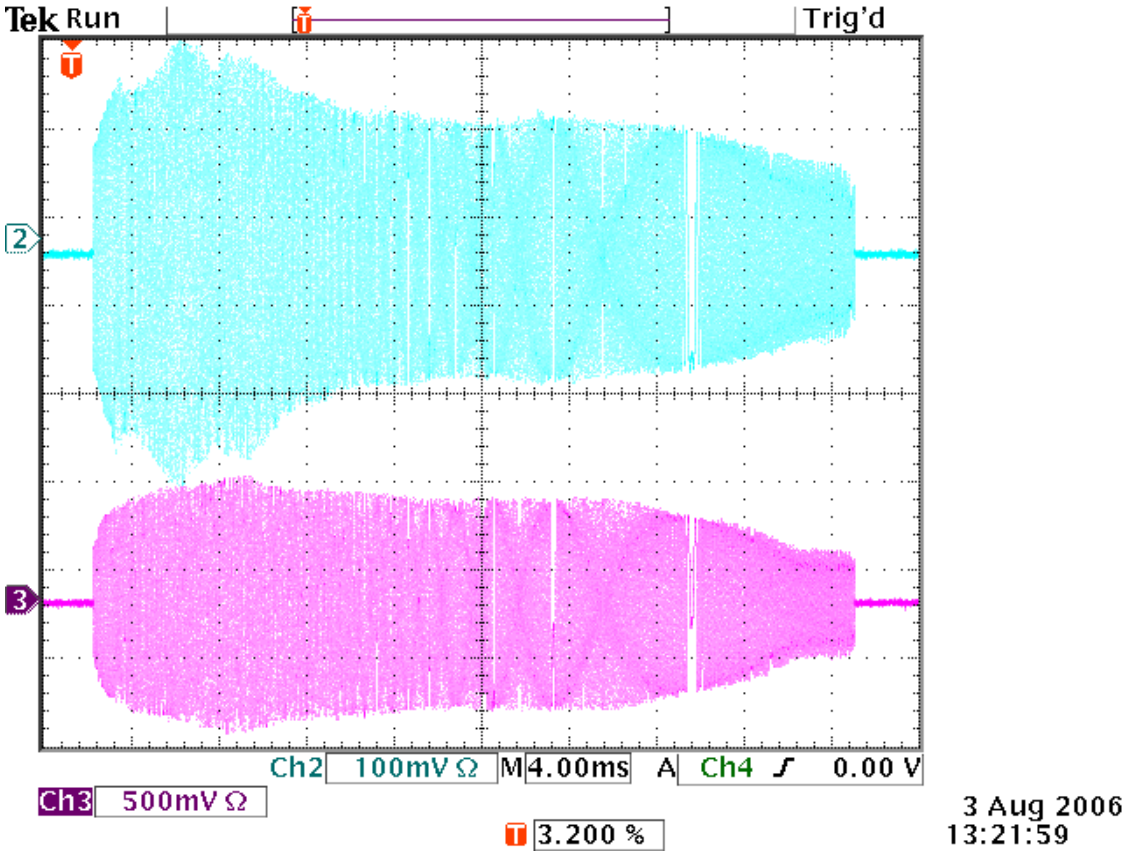

Figure 15: Cathode and anode raw signals viewed through RF monitors

- **General hardware configuration of the device**

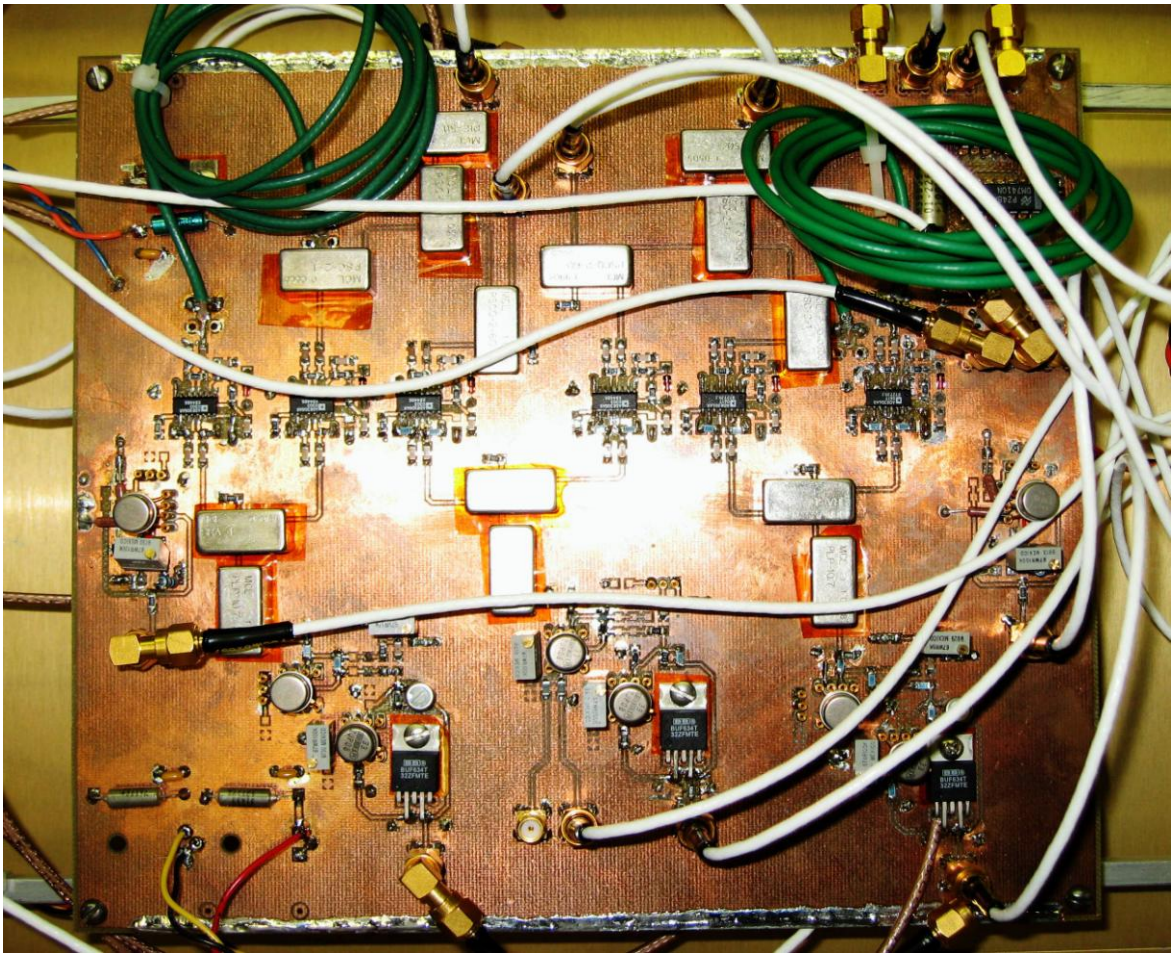

Figure16: Prototype board of the module

Device assembly and enclosure

Figure 17 : Front Panel of the device

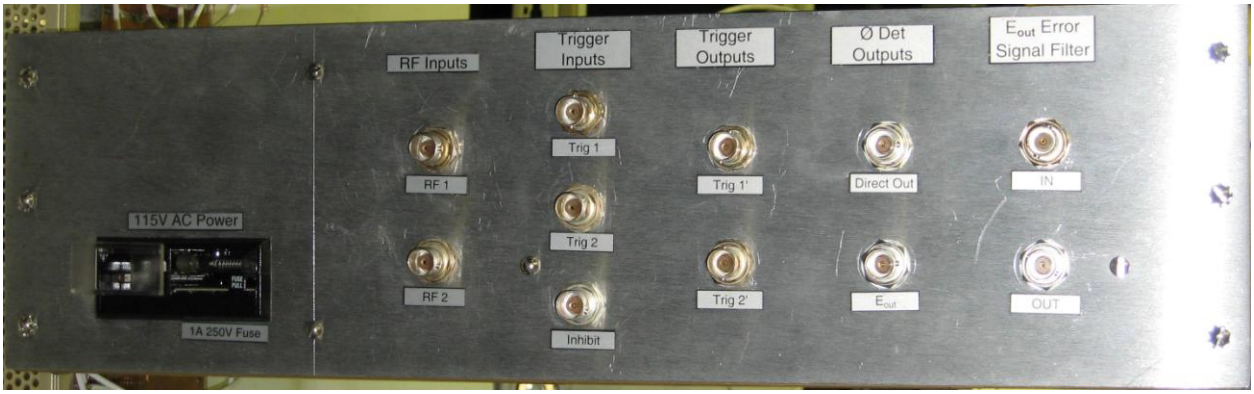

Figure 18 : Rear panel of the device

Conclusion

Keeping the cavity tuned in the RF Booster system for particles acceleration in a very important process taking place in the RF Booster which sometimes requires the signal to be monitored in different kind of aspects and this, most of the time preferable on a real time basis without having to rely too much on control computers. Our module comes as a very powerful diagnostic tool that can really enable a better, quick and real-time signal monitoring during measurement and troubleshooting operations. Overall, our design proved to be successful since we were able to test it in the RF Booster and generate quite satisfactory results. Also, this enhanced phase detector could eventually be used for measuring the phase error between the accelerating field and the beam. However, since our design was a prototype based one, it has not yet got to a definitive version, and some extra or complementary work still has to be done in order to come up with a very accurate and operational device ready to be adopted.

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Appendixes

1- Circuit diagram of the phase detector

2- Bill of material